Data Sheet For SD Memory Slave Controller

FPGA Implementation

iW-EMDMC-DS-01
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1. General Description

The SD Memory Slave controller is designed to resides within SD Memory and SDIO card. It serve as a Interface between SD bus and user application logic that provides actual function to the card. The SD memory Slave Controller is targeted into Actel Smart fusion FPGA. This slave controller provides simple and general-purpose 8-bit interface to user application. This Supports 1-bit and 4-bit SD Mode and feature like CRC generation and checking for command, response and data transfer.

The SD Memory slave controller receives commands from the host through the SD Memory interface. The standard SD register set is also implemented within the slave controller and process by the core. This support all mandatory SD Command Classes. The user interface block interfaces SD slave controller and user application through a 8-bit general purpose user interface for data transfer. The user interface block has a separate FIFO for read and write data buffering. A WDT is implemented in the user logic to support timeout logic for user interface application transaction.

2. Features

Following are the main features of the SD Memory Slave Controller:

- Compliant with SD Physical Specification Version 2.00
- Supports 1-bit and 4-bit SD Mode
- Supports Standard and High Capacity operations
- Supports Default and High Speed Modes of operation
- Supports all mandatory slave registers set
- CID Register fields are configurable through header file
- Supports only Standard command set
- Supports all mandatory SD Command Classes
- Class 0(Basic Commands)
    - CMD0
    - CMD2
    - CMD3
    - CMD6
    - CMD7
    - CMD8
    - CMD9
    - CMD10
    - CMD12
    - CMD13
    - CMD15

- Class 2(Block Read Commands)
  - CMD16
  - CMD17
  - CMD18
- Class 4(Block Write Commands)
  - CMD16
  - CMD24
  - CMD25
- Class 5(Erase Commands)
  - CMD32
  - CMD33
  - CMD38
- Class 8(Application Specific)
  - CMD55
  - ACMD6
  - ACMD13
  - ACMD22
  - ACMD23
  - ACMD41
  - ACMD42
  - ACMD51
- Class 10(Switch Commands)
  - CMD6
- CRC7 checking/generation for Command/Response
- CRC16 checking/generation for Data transfer
- Support Maximum block length of 512 bytes
- Supports Single and Multiple block read and write data transfer
- Supports Partial and Misalign Block length option
- SD Memory only implementation
- IP provides simple and general-purpose 8-bit interface to user application
- Combo card features are not supported
- SPI Mode is not supported
- Card Lock/Unlock Operation is not supported.

3. Block Diagram

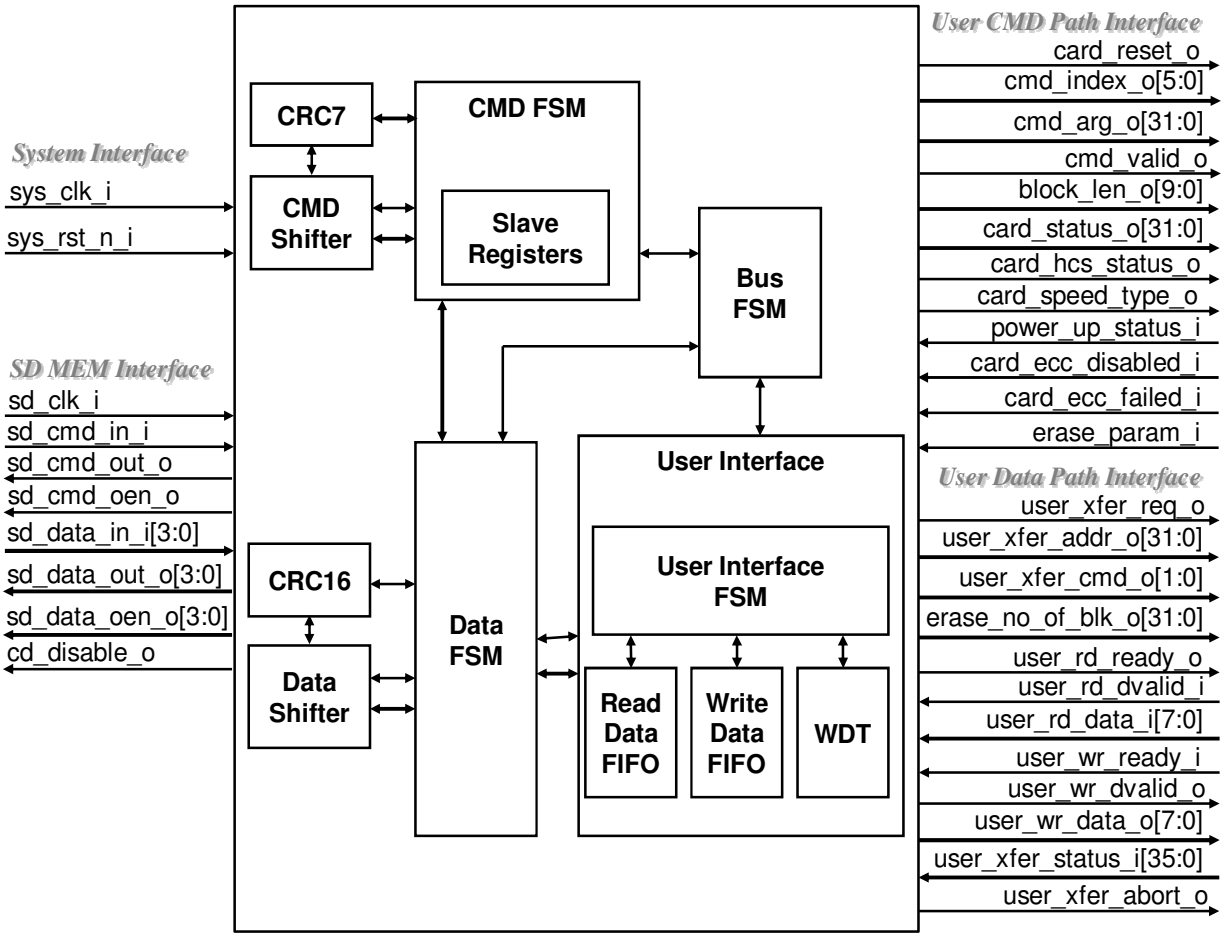

Figure 1: FPGA Block Diagram

4. Pinning Information

Table 1: System Interface IO Signal Description

Signal	Type	Width	Description
sys_rst_n_i	I	1	System Reset. Active Low Asynchronous reset input.

Signal	Type	Width	Description
sys_clk_i	I	1	System Clock. Clock input to the FPGA This clock is used for the user logic.

Table 2: SD Memory Interface IO Signal Description

Signal	Type	Width	Description
sd_clk_i	I	1	SDIO Bus Clock input.
sd_cmd_in_i	I	1	SDIO Command input
sd_cmd_out_o	O	1	SDIO Response output
sd_cmd_oen_o	O	1	SDIO Output enable
sd_data_in_i	I	4	SDIO Data input
sd_data_out_o	O	4	SDIO Data output
sd_data_oen_o	O	4	SDIO Data enable output
cd_disable_o	O	1	Connect/ Disconnect the 10K-90K ohm pull-up resistor The pull-up may be used for card detection. 0 → Connect 1 → Disconnect

Table 3: User Application Data Path Interface IO Signal Description

Signal	Type	Width	Description
user_xfer_req_o	O	1	User Application Request signal. For every new command user request is asserted for one clock cycle.

Signal	Type	Width	Description
user_xfer_addr_o[31:0]	O	32	User Application Address Output Standard Capacity Card -> It is in byte unit. High Capacity Card -> It is block (512 Byte) unit
user_xfer_cmd_o[1:0]	O	2	User Application Command Output 00 -> Erase Command 01 -> Erase and then Write Command 10 -> Write Command 11 -> Read Command
erase_no_of_blk_o[31:0]	O	32	Indicates no. of Block to be erased. This field is valid when user_xfer_cmd_o is “00” or “01”
user_rd_ready_o	O	1	User Application read ready signal. This signal indicates SD slave controller is ready to receive the data.
user_rd_dvalid_i	I	1	User Application read data valid signal. When valid data is available in user_rd_data_i bus, this is signal will be high.
user_rd_data_i[7:0]	I	8	User Application read data bus input SD Slave controller latch the user read data when user_rd_ready_o signal and user_rd_dvalid_i signal is high.
user_wr_ready_i	I	1	User Application Write ready input signal This signal indicates the user application is ready to receive the data.
user_wr_dvalid_o	O	1	User Application Write data valid output signal. SD Slave controller drive high when valid write data available on user_wr_data_o bus.
user_wr_data_o[7:0]	O	8	User Application Write data output bus.

Signal	Type	Width	Description
user_txfer_status_i[35:0]	I	36	User transfer status input [35] -> Erase successful [34] -> Erase failed [33] -> Write successful [32] -> Write failed [31:0] -> No. of blocks written successfully
user_xfer_abort_o	O	1	User transfer abort signal. When user application is responding for long time then slave controller will abort the current transfer cycle.

Table 4: User Application Command Path Interface IO Signal Description

Signal	Type	Width	Description
card_reset_o	O	1	Active high card reset output signal
cmd_index_o[5:0]	O	6	Received host command output
cmd_arg_o[31:0]	O	32	Received host command argument output
cmd_valid_o	O	1	Received host command valid output
block_len_o[9:0]	O	10	SD Block length output
card_status_o[31:0]	O	32	SD Slave card status register output
card_hcs_status_o	O	1	SD Slave card capacity type output 0 – SD Slave configured as standard Capacity Card 1 - SD Slave configured as high Capacity Card
card_speed_type_o	O	1	SD Slave card speed type output 0 – SD Slave operating in default speed (25MHz) 1 – SD Slave operating in high speed mode (50 MHz)

Signal	Type	Width	Description
power_up_status_i	I	1	Power Up Status input
card_ecc_disabled_i	I	1	Card ECC Disable Status input
card_ecc_failed_i	I	1	Card ECC Failed Status input
erase_param_i	I	1	Invalid Selection of write blocks for erase occured

5. Functional Description

The SD Memory Slave Controller is targeted into Actel Smart Fusion FPGA. The description of each blocks are listed below:

- **Command FSM:** The command path state machine controls the reception of Command and transmission of Response. Depending on the mode of operation, it generates appropriate control signals to the shifter and CRC7 block. It also parses the command received and generates suitable response output according to rules described in Specification, based on inputs from CRC7 block and Slave FSM. For every command, errors will be updated in the response flags of corresponding response.
- **Command Shifter:** The Command Transmitter and Response Receiver block has a 128-bit "Shift Register", it is used to receive and shift in the Command bits and transmit out the Response bits towards the Host. After it receives the complete command, it latches the value and passes it to the Command FSM for further processing. The incoming serial Command data is also passed to the CRC7 block to check for CRC. The serial Response data out is also passed to the CRC7 block to calculate CRC value. It appends the 7-bit CRC during response transmission.
- **CRC7:** The CRC7 module generates CRC Checksum for the 48-bit response generated by the SD Response Block. It calculates the CRC checksum for the start bit, transmission bit, command index and command argument (or card status). The CRC value computed crc7_calc_o is then shifted out after the response data when the crc7_shift_i is asserted by the SD Command FSM.
- **Slave FSM:** The SD slave Bus State Machine controls the overall operation of the SD memory controller operation. It defines the Bus States and their relations to SD Commands. The accepted commands indicated along with the individual states apply to SD Mode of operation.
- **Data FSM:** The Data FSM block controls the process of data being transmitted from the SD card to host during read operations or data being received by the SD card from the host during write operations.

- **Data Shifter:** The data Transmitter and Response Receiver block has a 8-bit "Shift Register". For data path, since SD operates in 4-bit mode or 1-bit mode, during transmission the data stored in the shifter is shifted out on bit by bit or 4-bit by 4-bit on data line/s. Similarly during reception, the data comes to the shifter bit by bit or 4-bit by 4-bit is shifted in and accumulate on it.
- **CRC16:** During data transmission, the CRC generator calculates CRC checksum for all data bits in a single block. When the Data FSM Module completes transmission of serial data it enables serial shifting of CRC16 value by asserting crc16_shift_i input. The same module acts as a CRC checker during data reception. CRC is calculated over the received data and CRC to result in a value of zero. For data in 4-bit mode, CRC16 is calculated separately for each data line.
- **User Interface:** The user interface block interfaces SD slave controller and user application through a 8-bit general purpose user interface for data transfer. The user application has a separate FIFO for read and write data buffering. A WDT is implemented in the user logic to implement system timeout logic for user interface transaction.

6. SD Memory Standard Slave Register Overview

The Register list of the SD Memory Slave Controller is as shown below.

Table 5: Register List

Sl. No	Registers	Width	Read/ Write	Address Offset
1.	Card Identification Register(CID)	128	R	-
2.	Relative Card Address Register(RCA)	16	R	-
3.	Card Specific Data Register (CSD) for storage capacity	128	R	-
4.	Card Specific Data Register (CSD) for High capacity	128	R	-
5.	SD Card Configuration Register (SCR)	64	R	-
6.	Operation Condition Register (OCR)	32	R	-
7.	SD Status Register (SSR)	512	R	-
8.	Card Status Register (CSR)	32	R	-

7. Timing Waveforms

Below waveforms shows the timing diagram of SD Memory Slave Controller.

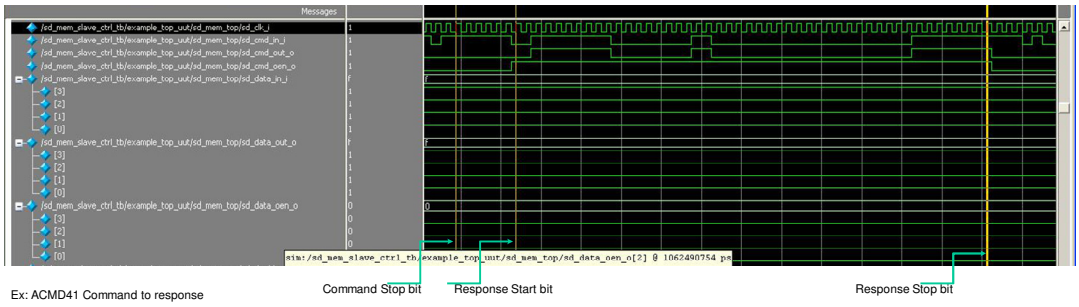

Figure 2: Command to Response Waveform

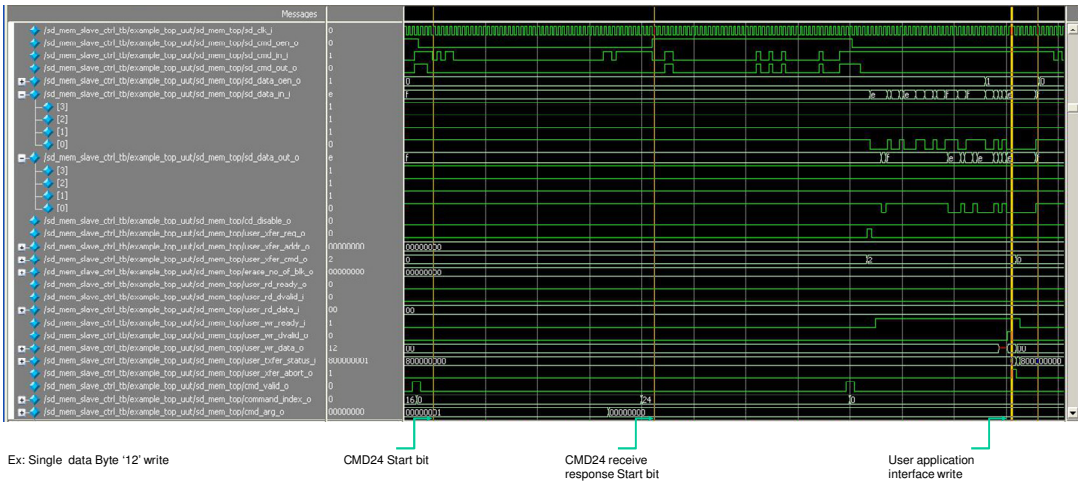

Figure 3: Single Block Write 1-bit Mode Waveform

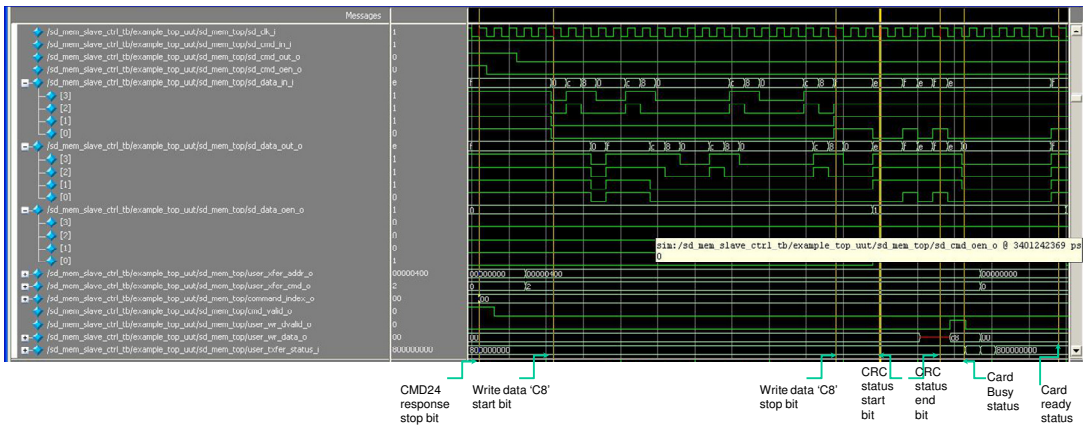

Figure 4: Single Block Write 4-bit Mode Waveform

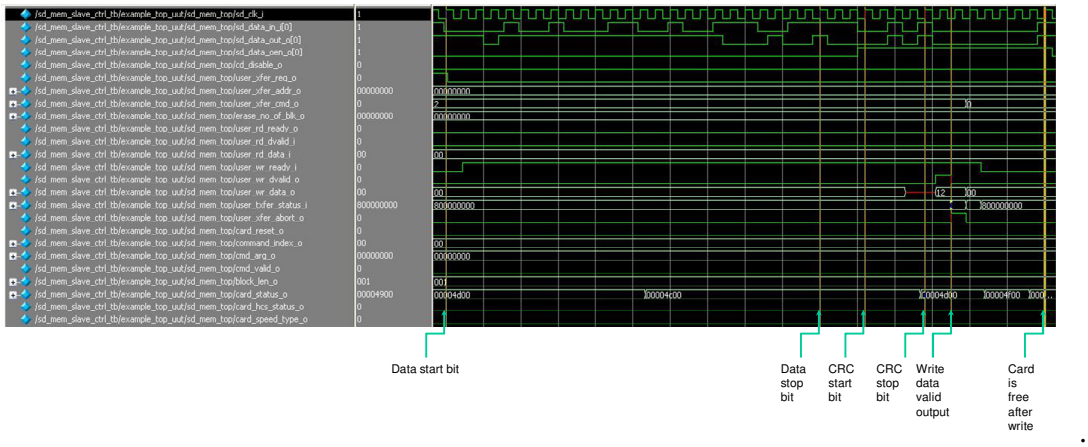

Figure 5: Single Block Write 1-bit Mode Waveform(User Interface)

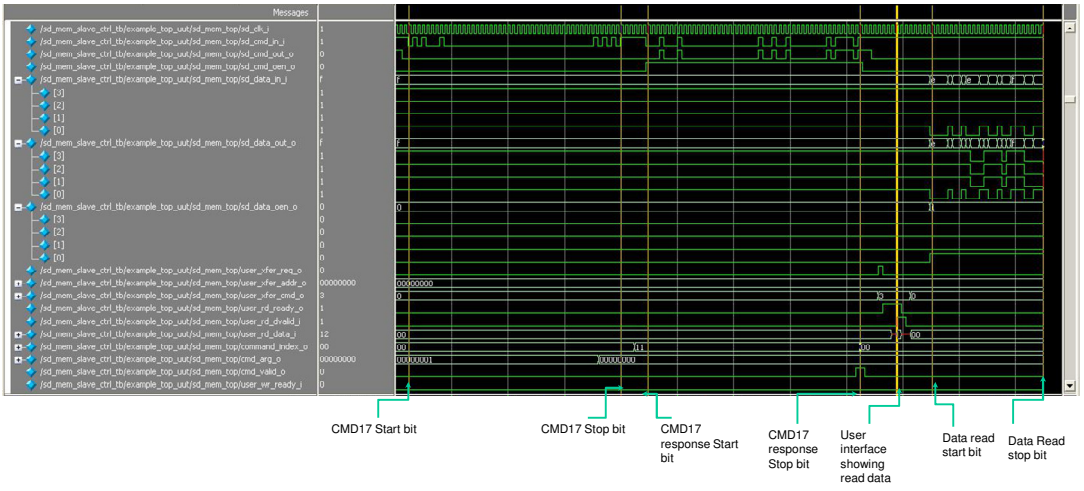

Figure 6: Single Block Read Waveform

8. Resource Utilization

The table below shows the utilization summary from the implementation of SD Memory Slave Controller for FPGA devices.

Table 6: Device Utilization Summary for Actel ProASIC3E

Logic Utilization	Used
Number of Core SEQ	2358
Number of Core COMB	3642
Number of RAM /FIFO Block	4
Number of IOs	220

Table 7: Device Utilization Summary for Xilinx Spartan-6

Logic Utilization	Used
Number of Slice Registers	1512
Number of Slice LUTs	1405
Number of RAMB8BWERs	2
Number of IOs	220

Table 8: Device Utilization Summary for Altera Cyclone IV E

Logic Utilization	Used
Number of Logic Elements combinational	1803
Number of Logic Elements registers	1496

Number of Memory bits	16384
Number of Pins	220

Table 9: Device Utilization Summary for Lattice ECP3

Logic Utilization	**Used**
Number of Slice	2503
Number of PIO	220